



SSC8022GS6B

N-Channel Enhancement Mode MOSFET

➤ Features

VDS	VGS	RDSON Typ.	ID
20V	±12V	51mR@4V5	3A
		65mR@2V5	

➤ Description

This device is produced with high cell density DMOS trench technology, which is especially used to minimize on-state resistance. This device particularly suits low voltage applications such as portable equipment, power management and other battery powered circuits, and low in-line power dissipation are needed in a very small outline surface mount package. Excellent thermal and electrical capabilities.

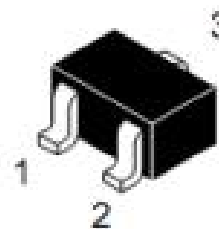
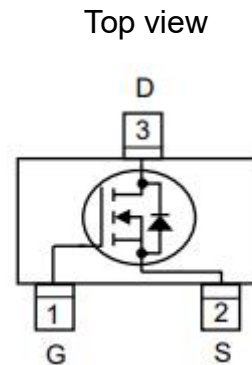
➤ Applications

- Load Switch
- Portable Devices
- DCDC conversion

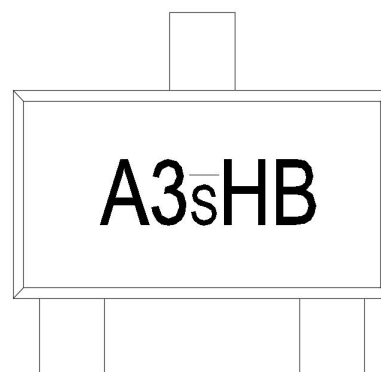
➤ Ordering Information

Device	Package	Shipping
SSC8022GS6B	SOT23	3000/Reel

➤ Pin configuration



SOT23



Marking



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	20	V
V_{GSS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current ^a	3	A
I_{DM}	Pulsed Drain Current ^b	10	A
P_D	Power Dissipation ^c	0.8	W
P_{DSM}	Power Dissipation ^a	0.45	W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		260	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		150	

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user is specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_{J(MAX)}=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

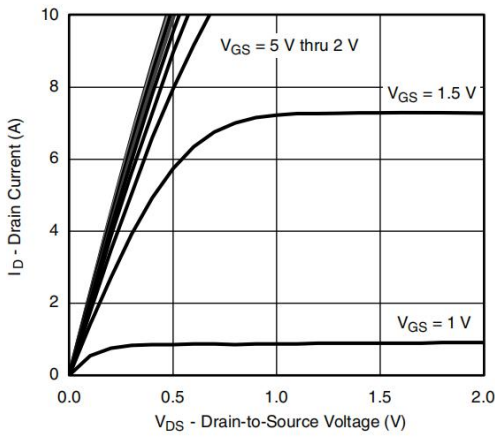


➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

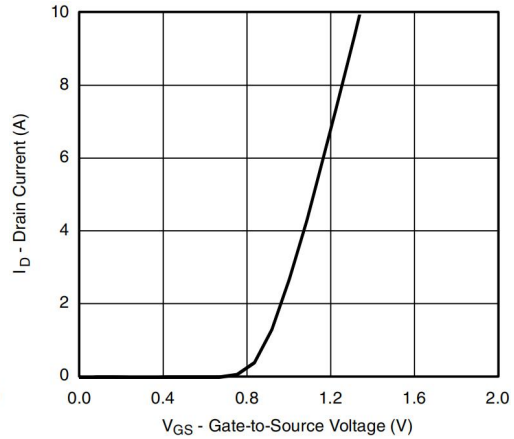
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4	0.7	1.2	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=4.5V, I_D=3.5A$		51	60	mR
		$V_{GS}=2.5V, I_D=3A$		65	85	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 12V, V_{DS}=0V$			± 100	nA
G_{FS}	Transconductance	$V_{DS}=5V, I_D=3.5A$		8	13	S
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=1.1A$		0.8	1.15	V
C_{iss}	Input Capacitance	$V_{DS}=10V, V_{GS}=0V, f=1MHz$		450		pF
C_{oss}	Output Capacitance			70		
C_{rss}	Reverse Transfer Capacitance			43		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=4.5V,$ $V_{DS}=5V, R_G=6R, I_D=3.5A$		6		ns
T_r	Rise Time			9		
$T_{D(OFF)}$	Turn-off delay time			18		
T_f	Fall Time			12		
Q_g	Total Gate charge	$V_{GS}=4.5V, V_{DS}=10V, I_D=3A$		11		nC
Q_{gs}	Gate to Source charge			1.1		
Q_{gd}	Gate to Drain charge			3.3		



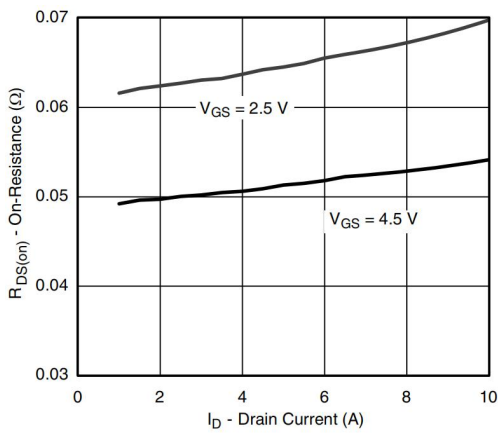
➤ Typical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)



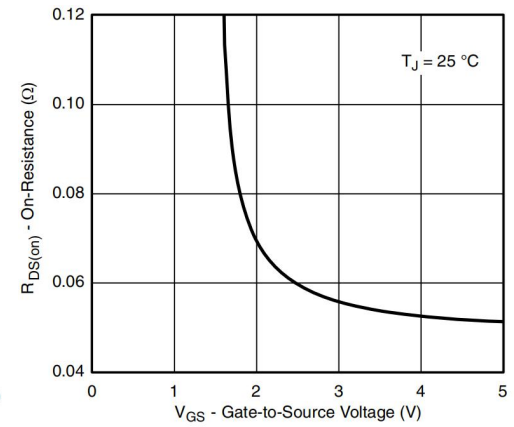
Output Characteristics



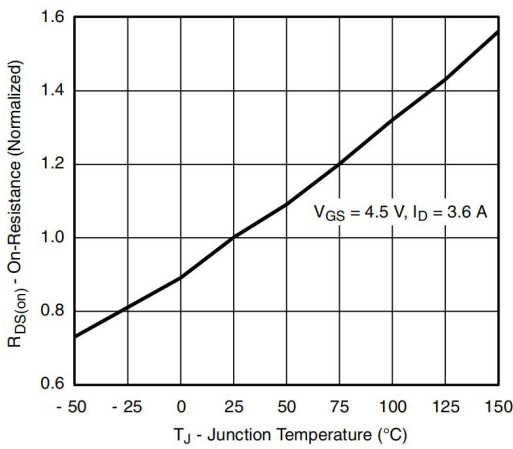
Transfer Characteristics



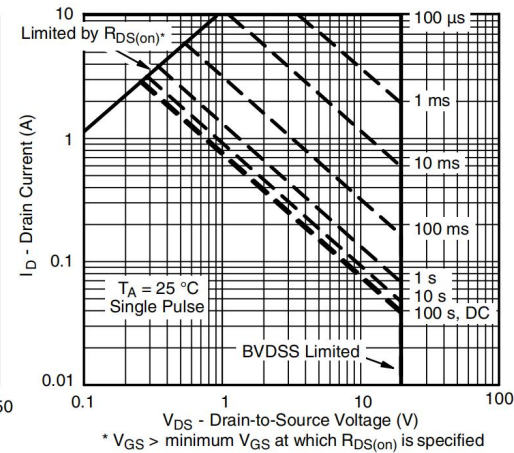
On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage



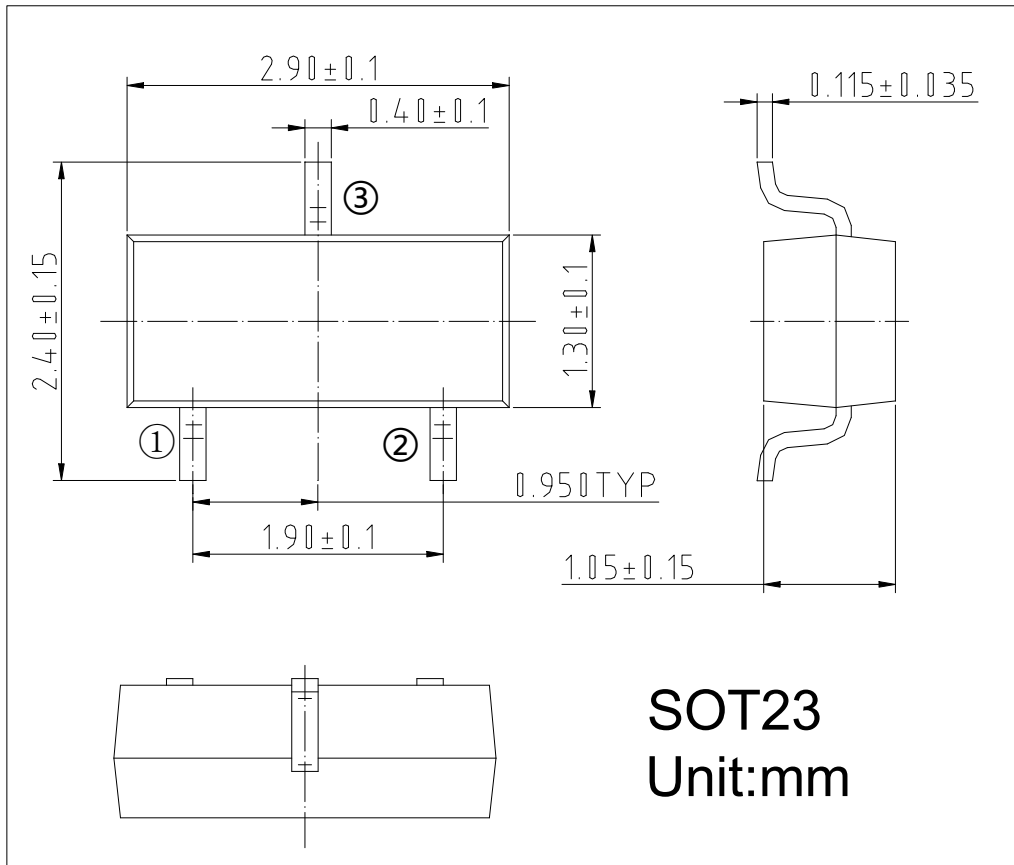
On-Resistance vs. Junction Temperature



Safe Operating Area, Junction-to-Ambient

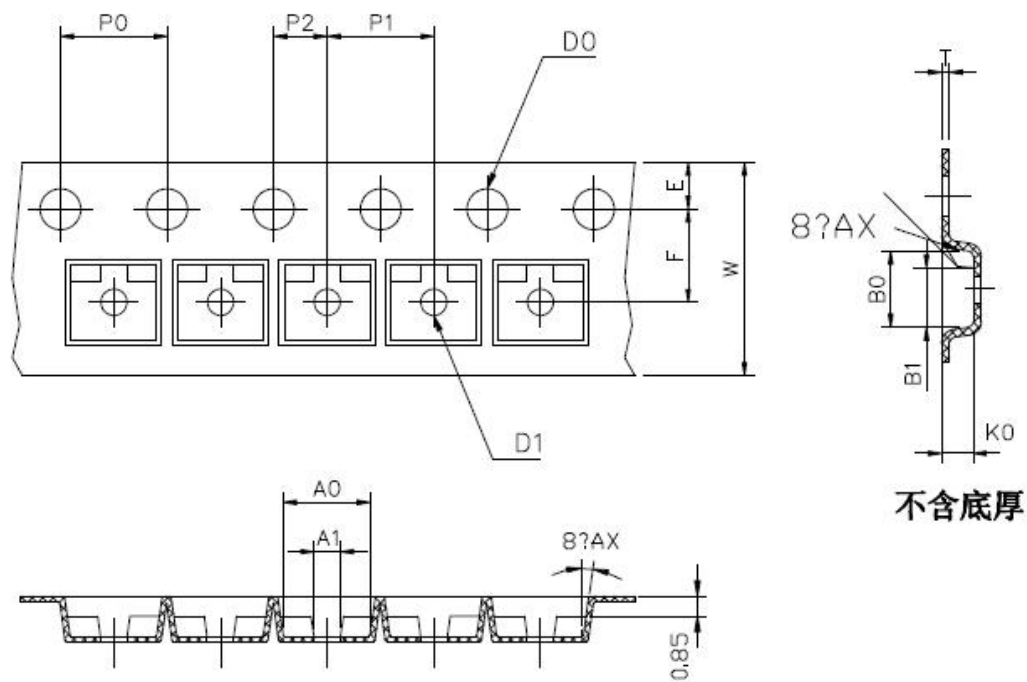


➤ Package Information





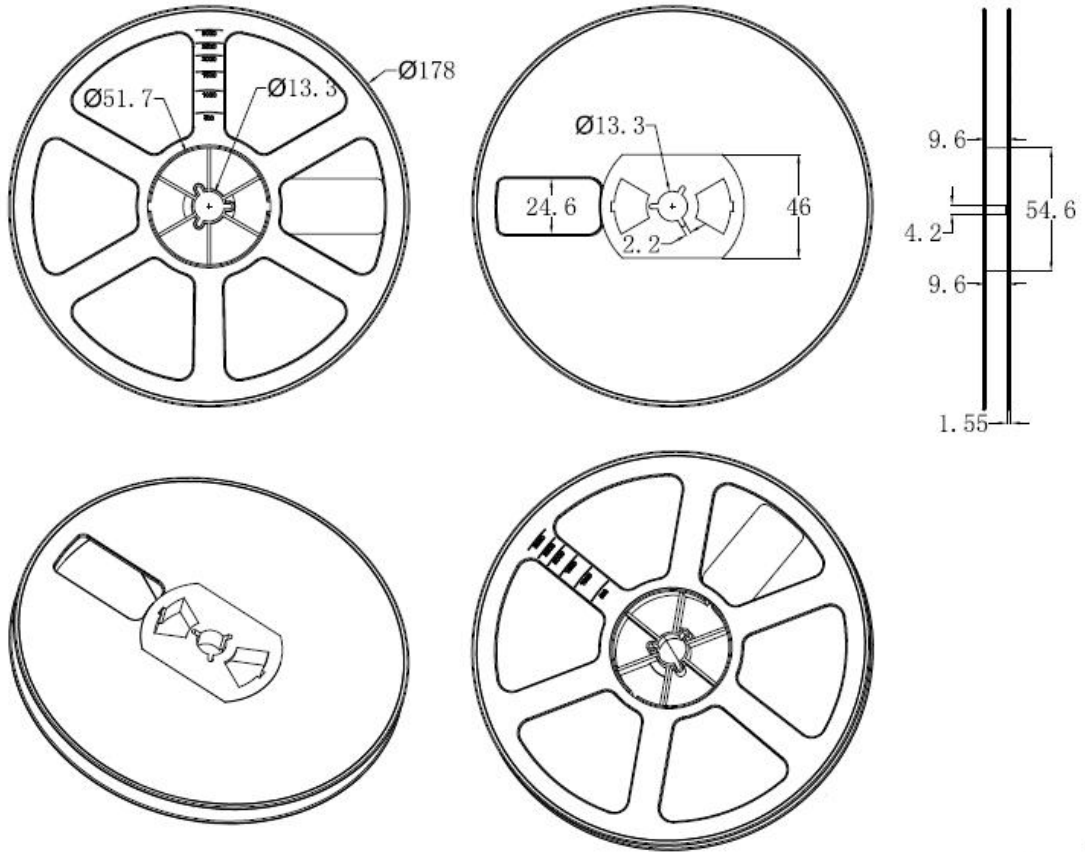
TAPE AND REEL DATA



Symbol	A0	A1	B0	B1	K0	D ₀	D ₁	P ₀	P ₁
Spec	3.15±0.10	1.15±0.10	2.80±0.10	2.15±0.10	1.30±0.10	1.55±0.10	1.10±0.10	4.00±0.10	4.00±0.10
Symbol	W	E	F	P ₂	t	t1	10*P ₀	4-P ₀	
Spec	7.95±0.05	1.70±0.05	3.50±0.10	2.00±0.10	0.21±0.02	0.05以上	40.00±0.10	4.00±0.10	

NOTE:

- 1.材料: PC+PS导电
- 2:10个链孔的累积公差不能超过0.2MM;
- 3.250MM带子的扇形不得超过1MM;
- 4.按照EIA-481-D的要求。





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