



## SSC8122GS8

### N-Channel Enhancement Mode MOSFET with ESD Protection

#### ➤ Features

VDS	VGS	RDS(on) Typ.	ID	ESD
20V	±8V	220mR@4V5	1.2A	2K
		270mR@2V5		
		340mR@1V8		

#### ➤ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

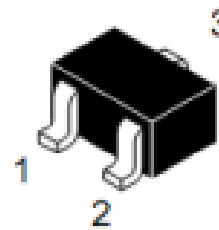
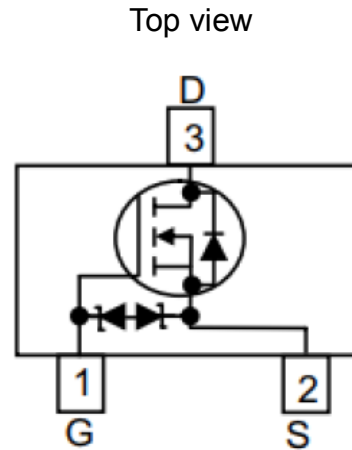
#### ➤ Applications

- Replace Digital Transistor
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching cell Phones

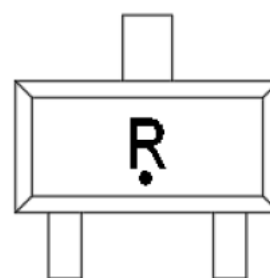
#### ➤ Ordering Information

Device	Package	Shipping
SSC8122GS8	SOT523	3000/Reel

#### ➤ Pin configuration



SOT523



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 8$	V
$I_D$	Continuous Drain Current <sup>a</sup>	1.2	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	3.6	A
$P_D$	Power Dissipation <sup>c</sup>	0.37	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	0.22	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		568	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		340	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_J(\text{MAX})=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

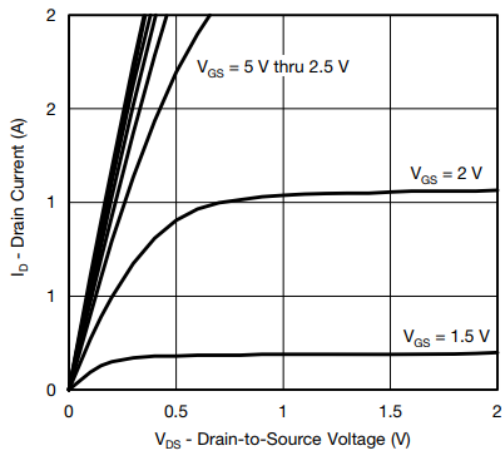


➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

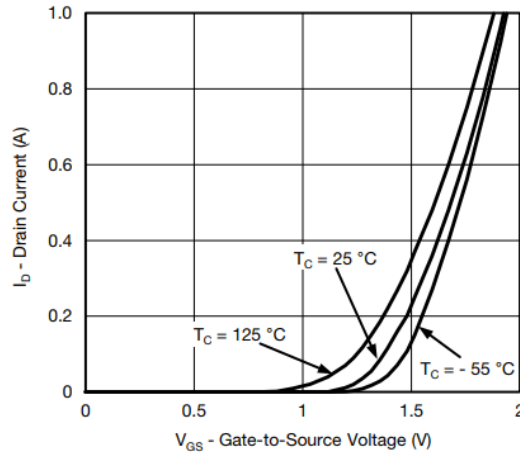
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.7	0.9	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=4.5V, I_D=0.5A$		220	400	mR
		$V_{GS}=2.5V, I_D=0.5A$		270	500	
		$V_{GS}=1.8V, I_D=0.35A$		340	800	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 8V, V_{DS}=0V$			$\pm 10$	$\mu A$
$G_{FS}$	Forward Transconductance	$V_{DS}=10V, I_D=0.4A$		1		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=0.5A$			1.3	V
$C_{iss}$	Input Capacitance	$V_{DS}=10V, V_{GS}=0V,$ $F=100KHZ$		88		pF
$C_{oss}$	Output Capacitance			17		
$C_{rss}$	Reverse Transfer Capacitance			9		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=4.5V,$ $V_{DD}=10V, R_G=6R,$ $I_D=0.55A$		22		ns
$T_{D(OFF)}$	Turn-off delay time			36		



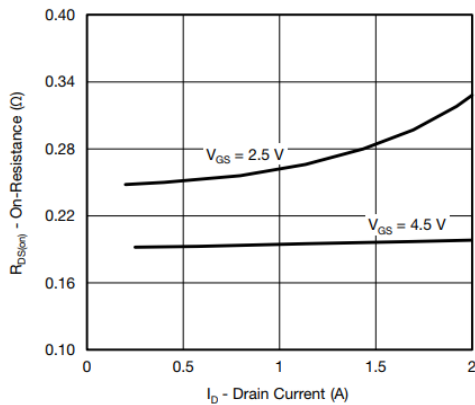
➤ **Typical Characteristics**( $T_A=25^\circ\text{C}$  unless otherwise noted)



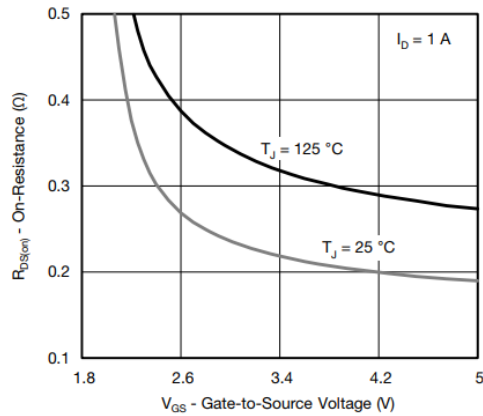
**Output Characteristics**



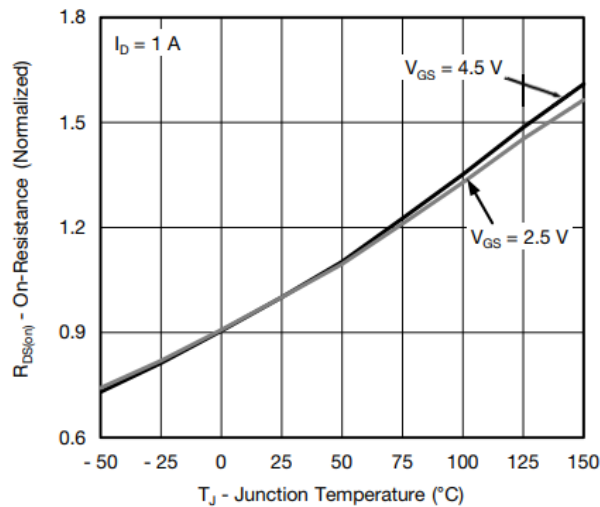
**Transfer Characteristics**



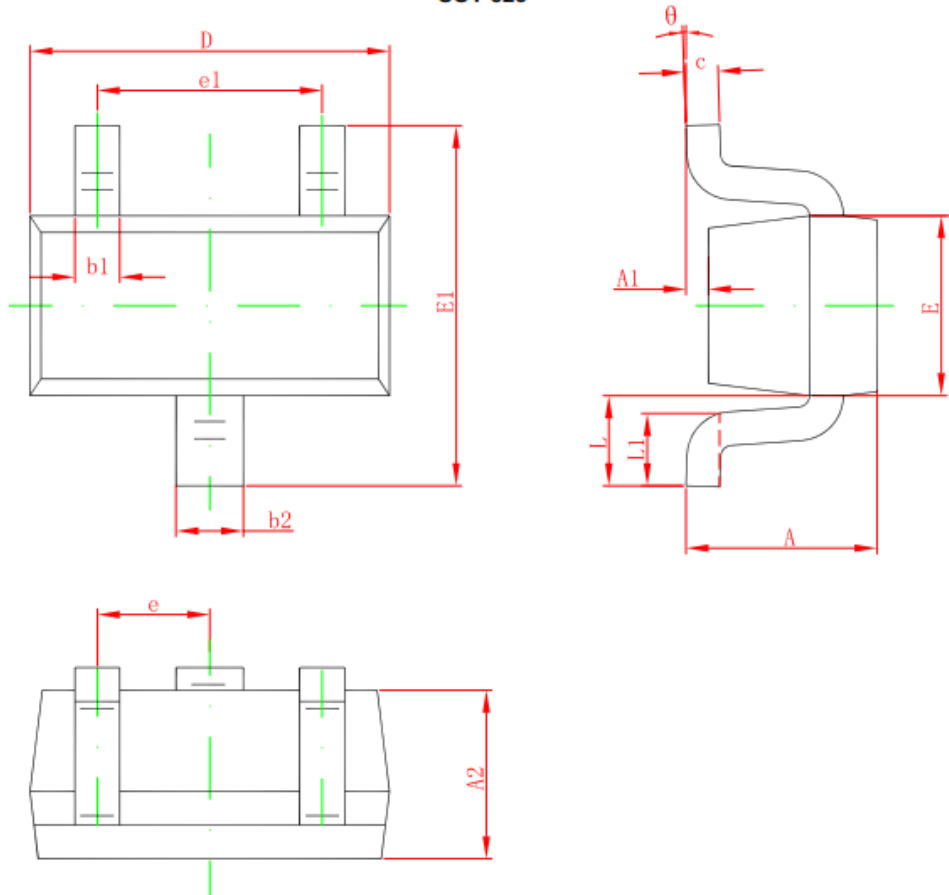
**On-Resistance vs. Drain Current and Gate Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**On-Resistance vs. Junction Temperature**

**➤ Package Information**
**SOT-523**


Symbol	Dimension in Millimeters	
	Min.	Max.
A	0.700	0.900
A1	0.000	0.100
A2	0.700	0.800
b1	0.150	0.250
b2	0.250	0.350
c	0.100	0.200
D	1.500	1.700
E	0.700	0.900
E1	1.450	1.750
e	0.500 Typ.	
e1	0.900	1.100
L	0.400 Ref.	
L1	0.260	0.460
$\theta$	0°	8°



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