



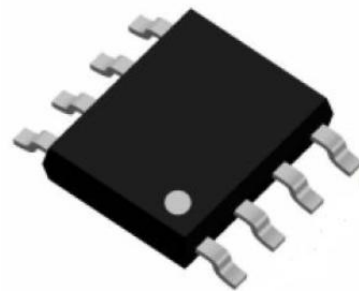
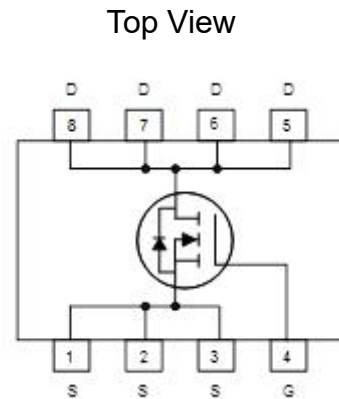
# SSC8030GS1

## N-Channel Enhancement Mode MOSFET

### ➤ Features

VDS	VGS	RDSON Typ.	ID
30V	±20V	9mR@10V	13A
		11mR@4V5	

### ➤ Pin configuration



SOP8

### ➤ Description

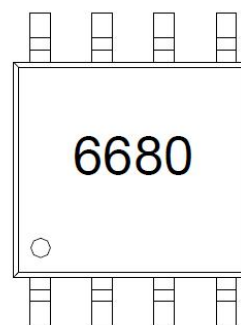
This device uses advanced trench technology to provide excellent RDSON and low gate charge. This device is suitable for use as a load switch or in PWM applications.

### ➤ Applications

- Load Switch
- NB/PC
- DCDC conversion

### ➤ Ordering Information

Device	Package	Shipping
SSC8030GS1	SOP8	2500/Reel



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

<b>Symbol</b>	<b>Parameter</b>	<b>Ratings</b>	<b>Unit</b>
$V_{DSS}$	Drain-to-Source Voltage	30	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current <sup>a</sup>	13	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	51	A
$P_D$	Power Dissipation <sup>c</sup>	6	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	2.5	W
$I_{AS}$	Avalanche Current <sup>b</sup> L=0.5mH Single Pulse	19	A
$E_{AS}$	Avalanche Energy <sup>b</sup> L=0.5mH Single Pulse	90	mJ
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

<b>Symbol</b>	<b>Parameter</b>	<b>Ratings</b>	<b>Unit</b>
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>	45	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	20	$^{\circ}\text{C}/\text{W}$

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_J(\text{MAX})=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

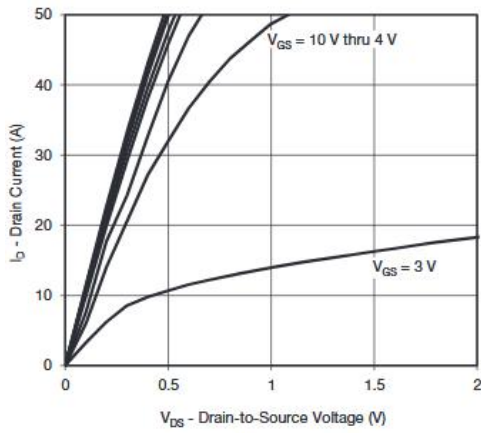


➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

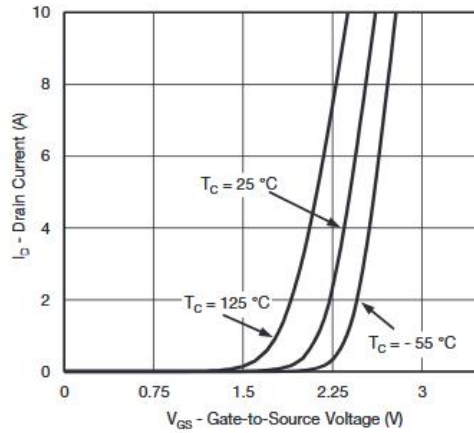
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=15A$		9	11	mR
		$V_{GS}=4.5V, I_D=12A$		11	15	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			$\pm 100$	nA
$G_{FS}$	Transconductance	$V_{DS}=15V, I_D=12A$		46		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=1A$		0.8	1.5	V
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		1200		pF
$C_{oss}$	Output Capacitance			200		
$C_{rss}$	Reverse Transfer Capacitance			105		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=10V,$ $V_{DS}=15V, R_L=2.3R, R_G=3R$		18		ns
$T_r$	Rise time			6		
$T_{D(OFF)}$	Turn-off delay time			70		
$T_f$	Fall time			17		
$Q_g$	Total Gate charge	$V_{GS}=10V, V_{DS}=10V, I_D=14A$		20		nC
$Q_{gs}$	Gate to Source charge			3		
$Q_{gd}$	Gate to Drain charge			5		



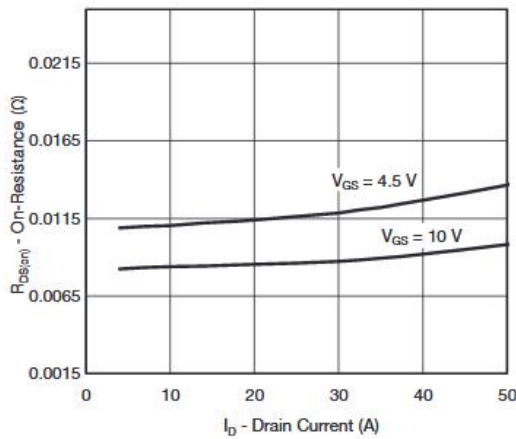
➤ **Typical Characteristics** ( $T_A=25^\circ\text{C}$  unless otherwise noted)



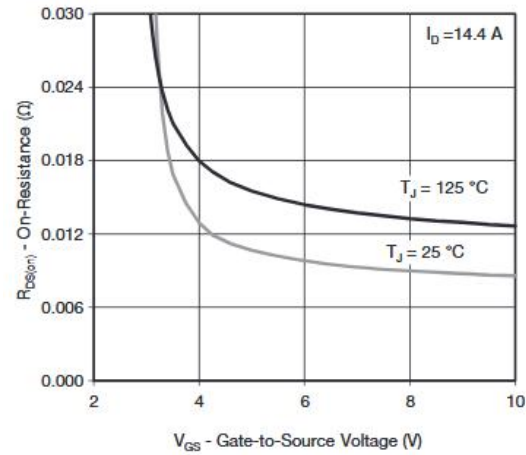
**Output Characteristics**



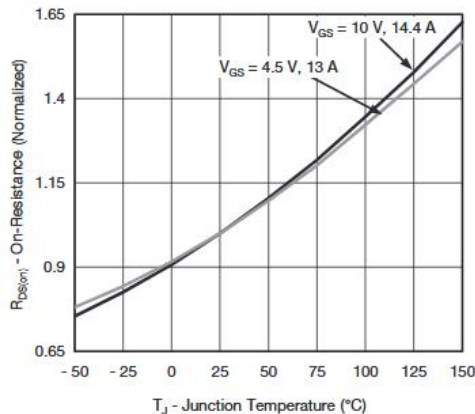
**Transfer Characteristics**



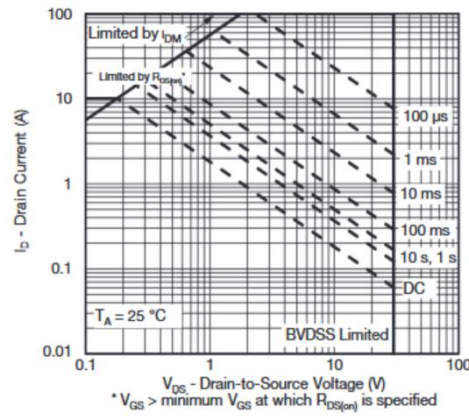
**On-Resistance vs. Drain Current**



**On-Resistance vs. Gate-to-Source Voltage**



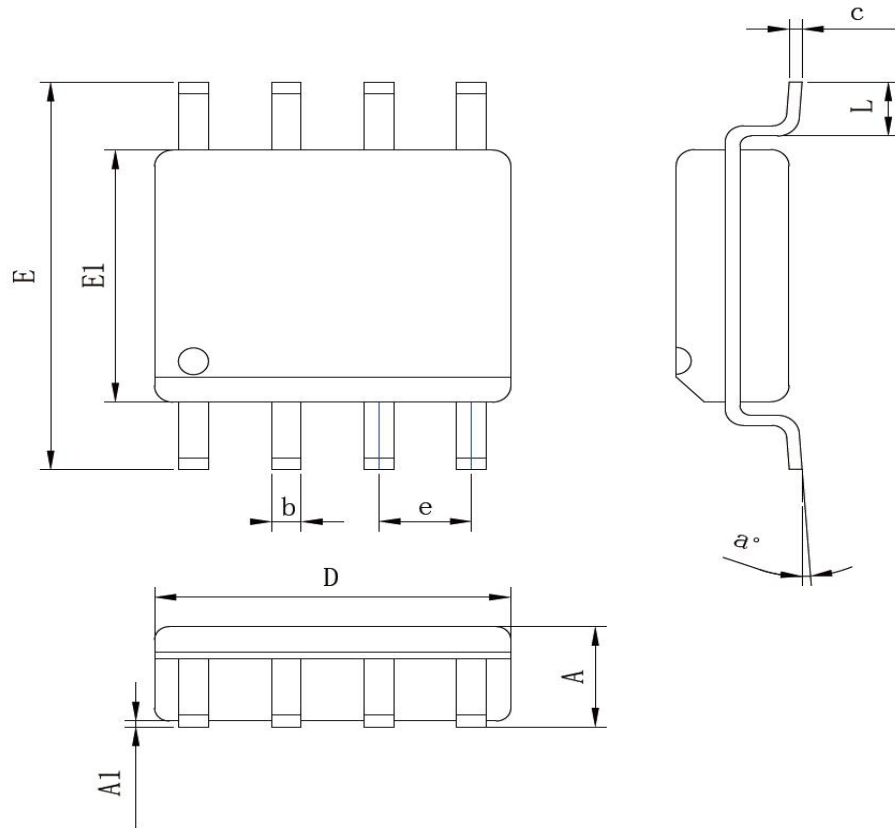
**On-Resistance vs. Junction Temperature**



**Safe Operating Area, Junction-to-Ambient**



➤ Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.75
A1	0.10	--	0.23
b	0.35	--	0.48
c	0.19	--	0.25
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.9	4.10
e	1.27BSC		
L	0.50	--	0.80
a°	0°	--	8°

**➤ History Version**

V1.0	Product datasheet release	2012-10-25
V2.0	The new vision updates Rjc to RjL	2020-06-05
V3.0	Update $P_D$ 、 $P_{DSM}$ 、 $I_{AS}$ and $E_{AS}$	2021-12-05

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