



## SSC8122GN1

### N-Channel Enhancement Mode MOSFET with ESD protection

#### ➤ Features

VDS	VGS	RDSON Typ.	ID	ESD
20V	±8V	195mR@4V5	1.1A	2K
		240mR@2V5		
		305mR@1V8		

#### ➤ Description

This device is a N-Channel enhancement mode MOSFET which is produced with high cell density and DMOS trench technology. This device particularly suits low voltage applications, especially for battery powered circuits, the tiny and thin outline saves PCB consumption.

#### ➤ Applications

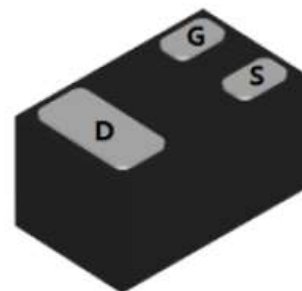
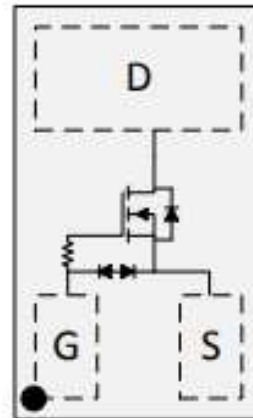
- Load Switch
- Portable Devices

#### ➤ Ordering Information

Device	Package	Shipping
SSC8122GN1	DFN1006	10K/Reel

#### ➤ Pin configuration

Top view



Bottom View



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	20	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 8$	V
$I_D$	Continuous Drain Current <sup>a</sup>	1.1	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	3.1	A
$P_D$	Power Dissipation <sup>c</sup>	0.32	W
$P_{DSM}$	Power Dissipation <sup>a</sup>	0.18	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>		690	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		379	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

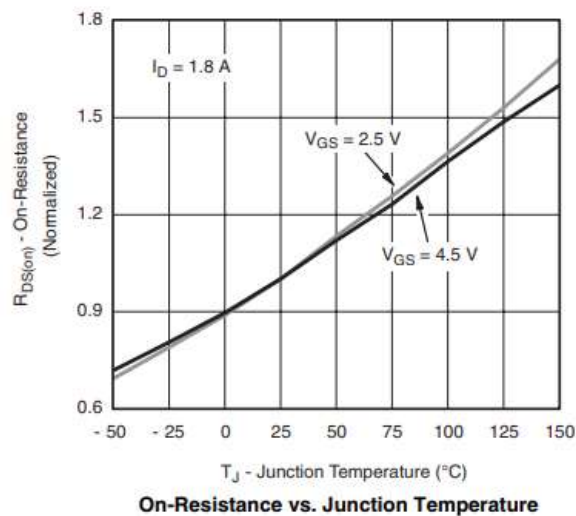
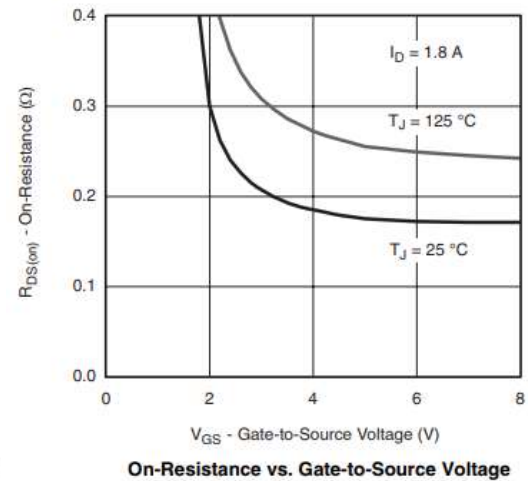
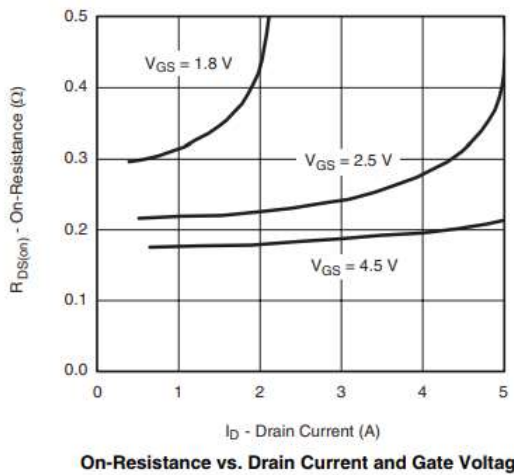
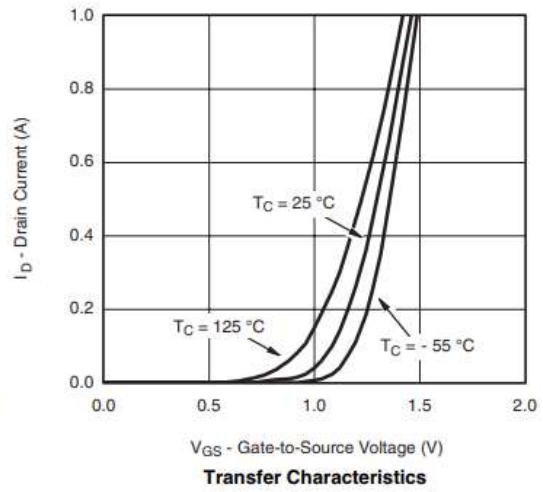
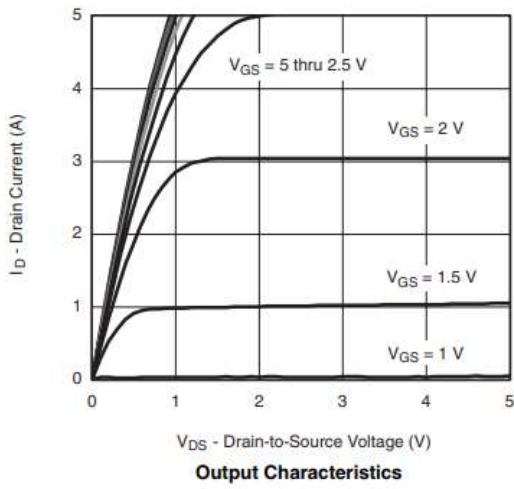


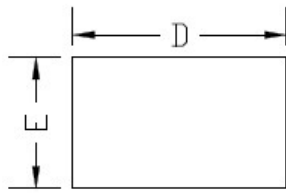
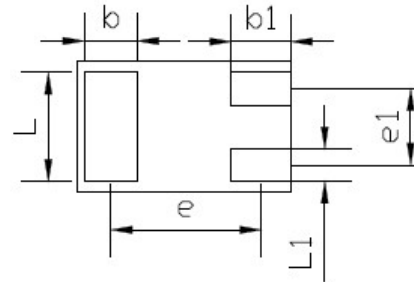
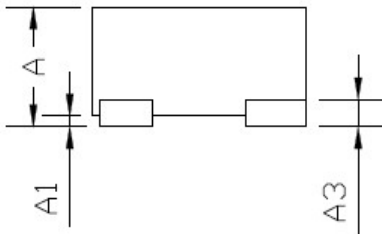
➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	0.68	1	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=4.5V, I_D=0.5A$		195	310	mR
		$V_{GS}=2.5V, I_D=0.5A$		240	380	
		$V_{GS}=1.8V, I_D=0.35A$		305	800	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=20V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 8V, V_{DS}=0V$			$\pm 10$	$\mu A$
$G_{FS}$	Transconductance	$V_{DS}=5V, I_D=0.5A$		2		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=0.5A$		0.7	1.3	V
$C_{iss}$	Input Capacitance	$V_{DS}=10V, V_{GS}=0V,$ $f=1MHz$		66		pF
$C_{oss}$	Output Capacitance			18		
$C_{rss}$	Reverse Transfer Capacitance			9		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=4.5V,$ $V_{DS}=10V, R_G=6R, I_D=0.6A$		20		ns
$T_r$	Rise time			13		
$T_{D(OFF)}$	Turn-off delay time			40		
$T_f$	Fall time			12		

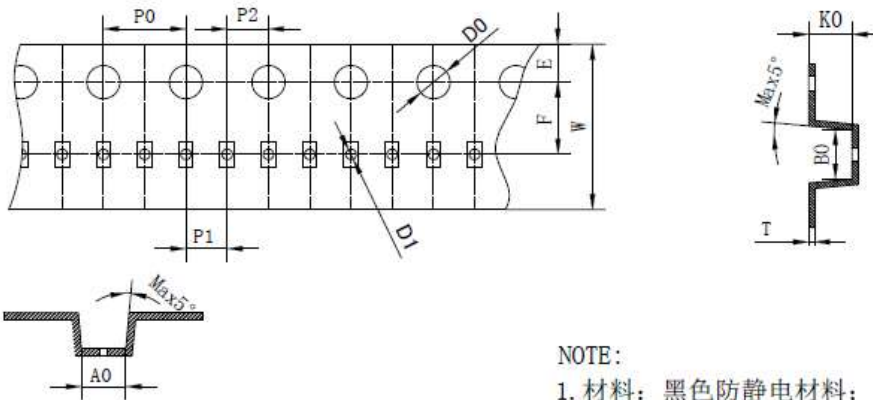


➤ **Typical Characteristics**( $T_A=25^\circ\text{C}$  unless otherwise noted)



**➤ Package Information**
**POD**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

COMMON DIMENSION (MM)			
PKG	DFN1006		
REF.	MIN.	NOM.	MAX
A	>0.4	-	0.50
A1	0.00	-	0.05
A3	0.125REF.		
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b	0.20	0.25	0.30
b1	0.20	0.30	0.40
L	0.45	0.50	0.55
L1	0.10	0.15	0.20
e	0.675		
e1	0.35		

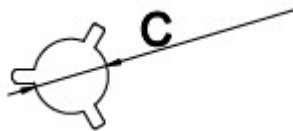
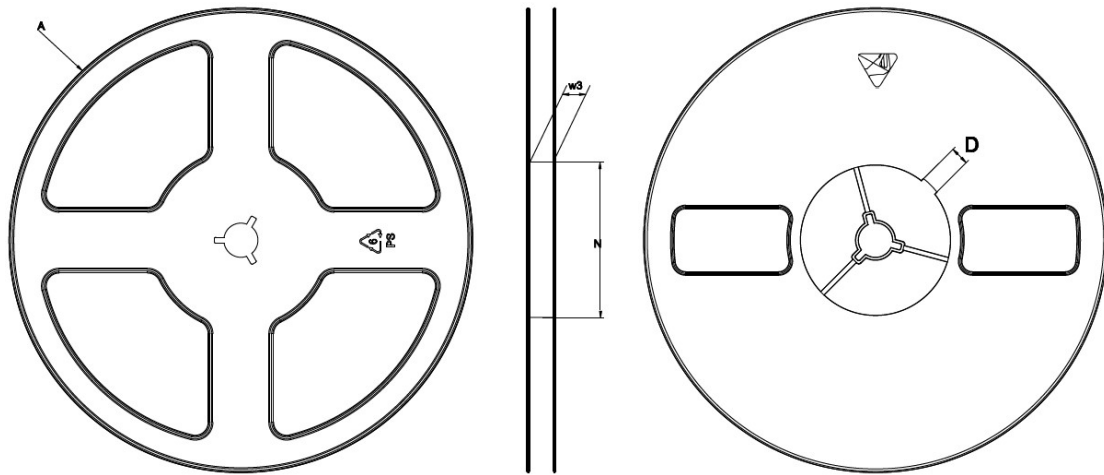
**Tape Data**

**NOTE:**

1. 材料：黑色防静电材料；
2. 10个链孔的累积公差不能超过±0.2
3. 尺寸符合EIA-481-E的要求。

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	0.69±0.05	1.15±0.05	0.60±0.05	4.00±0.10	2.00±0.05	2.00±0.05
SYMBOL	T	E	F	D0	D1	W
SPEC	0.18±0.03	1.75±0.10	3.50±0.05	1.55±0.05	0.50±0.05	8.00 <sup>+0.3</sup> <sub>-0.1</sub>



Reel Data



材质说明：该产品用料为 PS

TYPE	A	N	C	D	w3
8MM	$\begin{matrix} +1 \\ \text{Ø178} \\ -1 \end{matrix}$	$\begin{matrix} +1 \\ \text{Ø60} \\ -1 \end{matrix}$	$\begin{matrix} +0,3 \\ \text{Ø13,3} \\ -0,3 \end{matrix}$	7,5±0,5	9±0.3



➤ **History Version**

V1.0	Product datasheet	2019-01-04
V2.1	Update $R_{DS(on)}$	2021-09-01

**DISCLAIMER**

AFSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. AFSEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICIENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

THE GRAPHS PROVIDED IN THIS DOCUMENT ARE STATISTICAL SUMMARIES BASED ON A LIMITED NUMBER OF SAMPLES AND ARE PROVIDED FOR INFORMATIONAL PURPOSE ONLY. THE PERFORMANCE CHARACTERISTICS LISTED IN THEM ARE NOT TESTED OR GUARANTEED. IN SOME GRAPHS, THE DATA PRESENTED MAY BE OUTSIDE THE SPECIFIED OPERATING RANGE (E.G. OUTSIDE SPECIFIED POWER SUPPLY RANGE) AND THEREFORE OUTSIDE THE WARRANTED RANGE.