SSC8633GSB

N- and P-Channel Complementary, MOSFET

➢ Features

N-Channel

VDS	VGS	RDSON Typ.	ID
30V	±16V	42mR@10V	3.6A
		46mR@4V5	
		56mR@2V5	

P-Channel

VDS	VGS	RDSON Typ.	ID
-30V	±12V	48mR@-10V	-3.2A
		55mR@-4V5	
		77mR@-2V5	

➢ Description

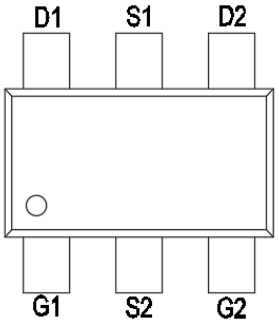
SSC8633GSB uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

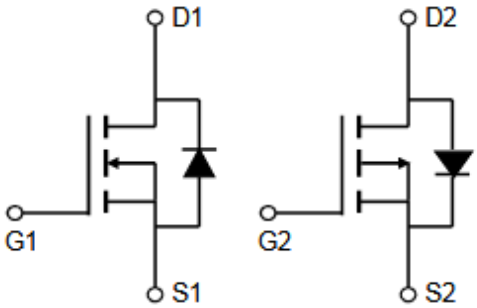
➢ Applications

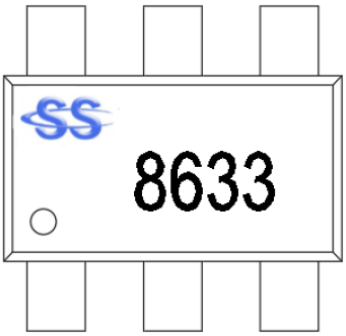
- Inverter
- CCFL Driver
- Half and Full Bridge Topology

➢ Pin configuration

Top view







Marking

➢ Ordering Information

Device	Package	Shipping
SSC8633GSB	SOT23-6L	3000/Reel

➢ Absolute Maximum Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter		N-Channel	P-Channel	Unit
V_{DSS}	Drain-to-Source Voltage		30	-30	V
V_{GSS}	Gate-to-Source Voltage		±12	±12	V
I_D	Continuous Drain Current [a]	TA=25℃	3.6	-3.2	A
		TA=70℃	2.2	-2	A
I_{DM}	Pulsed Drain Current [b]		14	-12	A
P_{DSM}	Power Dissipation [a]		2.4		W
P_D	Power Dissipation [c]	TA=25℃	1.2		W
		TA=70℃	0.75		W
T_J	Operation junction temperature		-55 to 150		℃
T_{STG}	Storage temperature range		-55 to 150		℃

➢ Thermal Resistance Ratings(T_A=25℃ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance [a]		105	℃/W
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		52	

Note:

a. The value of $R_{\theta JA}$ is measured with the device mounted on 1 in^2 FR-4 board with 2oz.copper,in a still air environment with T_A=25℃.The value in any given application depends on the user is specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

b. Repetitive rating, pulse width limited by junction temperature.

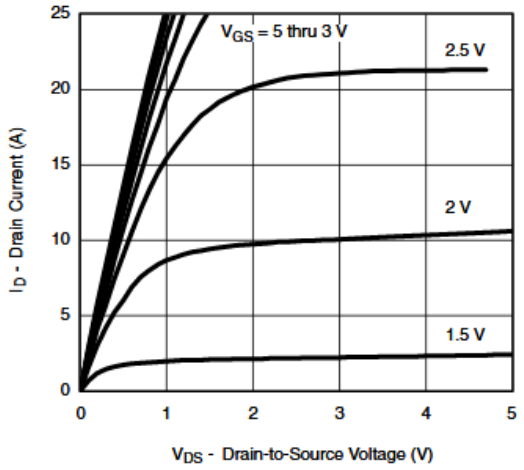
c. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

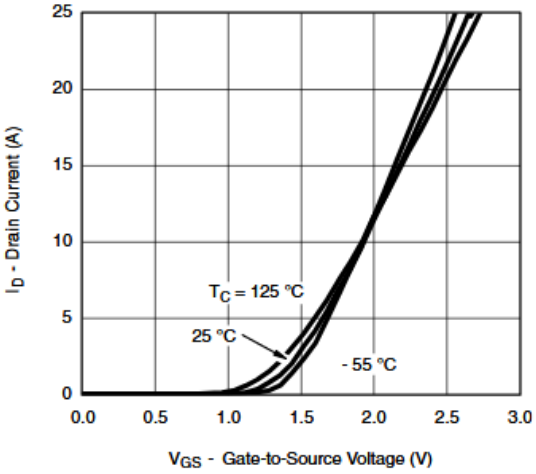
➢ **Electronics Characteristics**(T_A=25℃ unless otherwise noted)

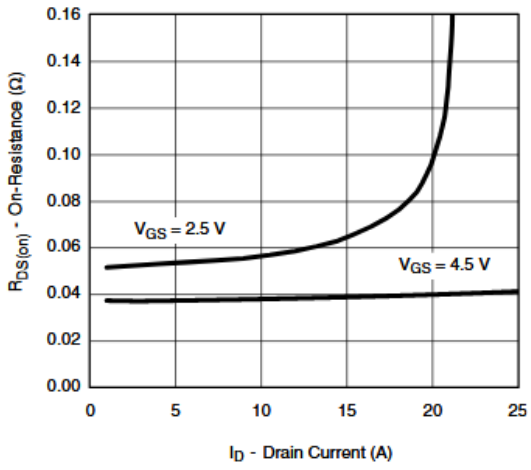
Symbol	Parameter	Test Conditions		Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	VGS=0V,ID=250uA	N-CH	30			V
		VGS=0V,ID=-250uA	P-CH	-30			
$V_{GS\ (th)}$	Gate Threshold Voltage	VDS=VGS,ID=250uA	N-CH	0.7	1	1.3	V
		VDS=VGS,ID=-250uA	P-CH	-0.6	-0.9	-1.3	
$R_{DS(on)}$	Drain-Source On-Resistance	VGS=10V,ID=3.6A	N-CH		42	55	mR
		VGS=10V,ID=-3.2A	P-CH		48	60	
		VGS=4.5V,ID=3A	N-CH		46	70	
		VGS=-4.5V,ID=-2A	P-CH		55	75	
		VGS=2.5V,ID=2A	N-CH		56	80	
		VGS=-2.5V,ID=-1.8A	P-CH		77	100	
I_{DSS}	Zero Gate Voltage Drain Current	VDS=24V,VGS=0V	N-CH			1	uA
		VDS=-24V,VGS=0V	P-CH			-1	
I_{GSS}	Gate-Source leak current	VGS=±16V,VDS=0V	N-CH			±100	nA
		VGS=±12V,VDS=0V	P-CH			±100	
G_{FS}	Forward Transconductance	VDS=5V,ID=2A	N-CH		10		S
		VDS=-5V,ID=-2A	P-CH		15		
V_{SD}	Forward Voltage	VGS=0V,IS=1A	N-CH		0.78	1.3	V
		VGS=0V,IS=-1A	P-CH		-0.77	-1.3	
Ciss	Input Capacitance	**NMOS:** VDS=15V, VGS=0V, f=1MHZ **PMOS:** VDS=-15V, VGS=0V, f=1MHZ	N-CH		510		pF
			P-CH		430		
Coss	Output Capacitance		N-CH		70		
			P-CH		60		
Crss	Reverse Transfer Capacitance		N-CH		45		
			P-CH		40		

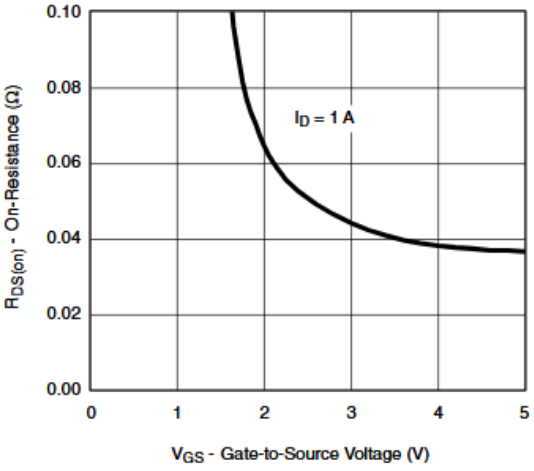
Qg	Total Gate Charge	**NMOS:** VDS=15V, VGS=4.5V, ID=4A **PMOS:** VDS=-15V, VGS=-4.5V, ID=-3A	N-CH		10		nC
			P-CH		9		
Qgs	Gate Source Charge		N-CH		2.2		
			P-CH		2.3		
Qgd	Gate Drain Charge		N-CH		1.1		
			P-CH		1.9		
$T_{D(ON)}$	Turn-on delay time	**NMOS:** VDS=15V, VGS=10V, RL=10R, RGEN=6R **PMOS:** VDS=-15V, VGS=-10V, RL=10R, RGEN=6R	N-CH		9		ns
			P-CH		13		
Tr	Rise time		N-CH		12		
			P-CH		15		
$T_{D(OFF)}$	Turn-off delay time		N-CH		26		
			P-CH		21		
Tf	Fall time		N-CH		18		
			P-CH		14		

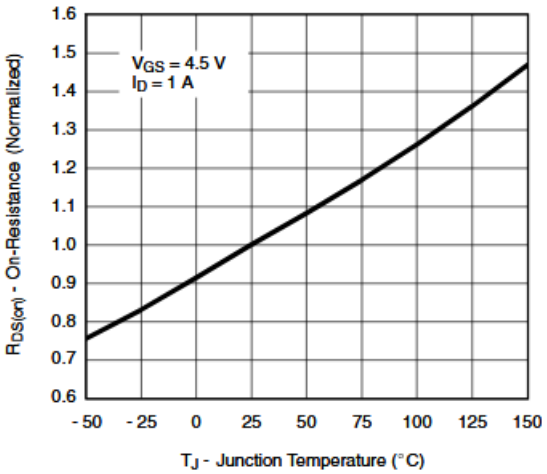
➢ N-Channel Typical Characteristics(T_A=25℃ unless otherwise noted)

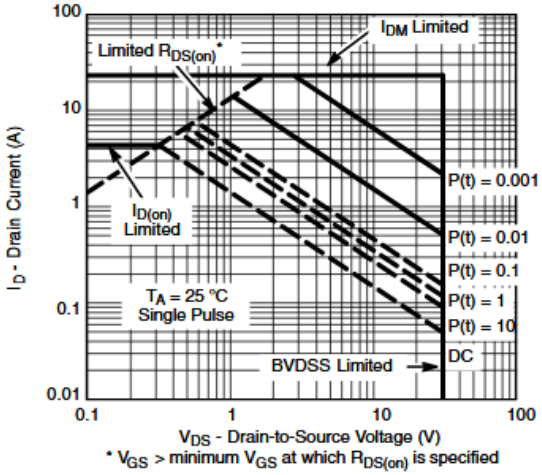




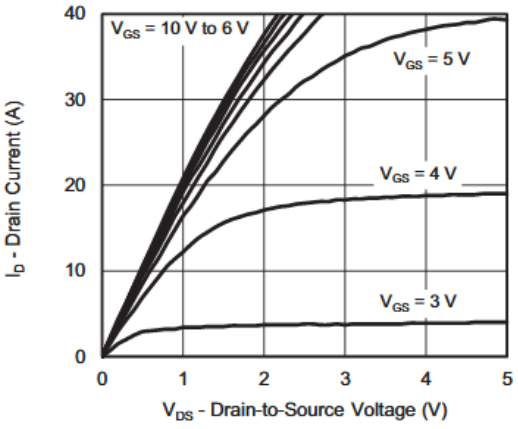




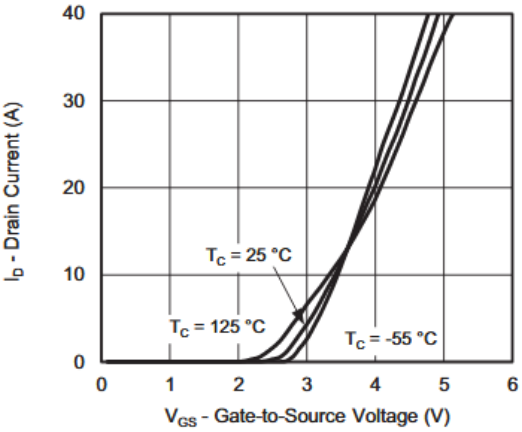




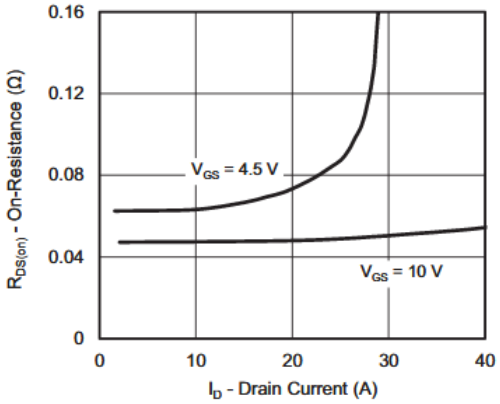
➢ P-Channel Typical Characteristics(T_A=25℃ unless otherwise noted)



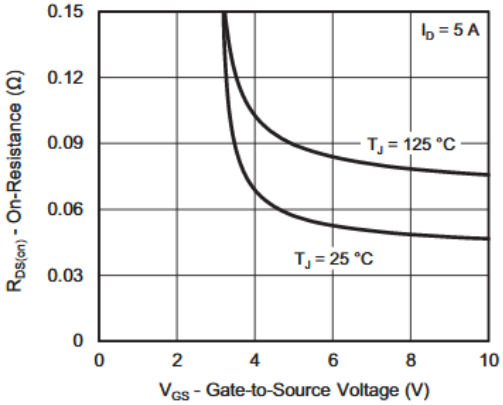
Output Characteristics



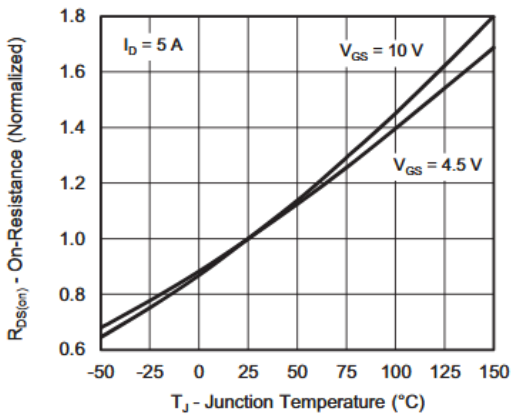
Transfer Characteristics



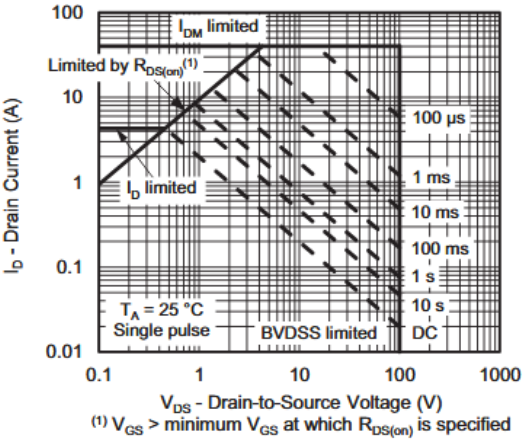
On-Resistance vs. Drain Current and Gate Voltage



On-Resistance vs. Gate-to-Source Voltage

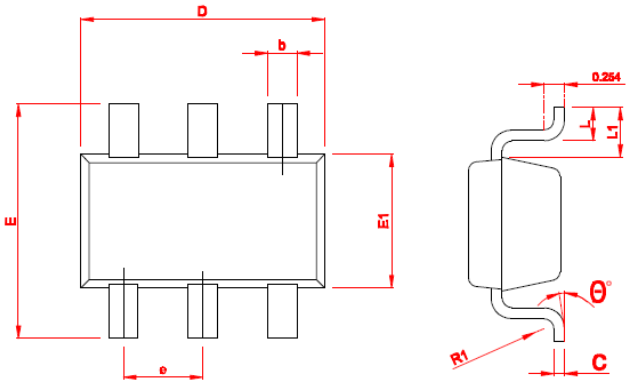


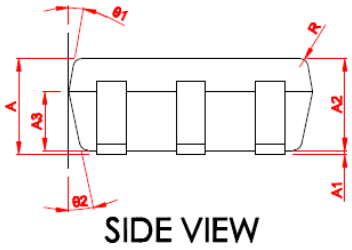
On-Resistance vs. Junction Temperature



Safe Operating Area, Junction-to-Ambient

➢ Package Information





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.15	1.24
* A1	0.01	0.05	0.09
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.117	0.127	0.157
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	0.90	0.95	1.00
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* θ	0	--	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

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