



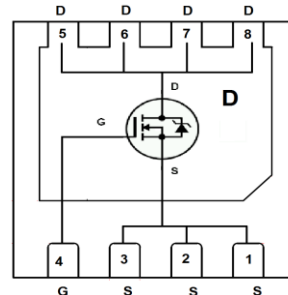
SSC8030GQ4

N-Channel Enhancement Mode MOSFET

➤ Features

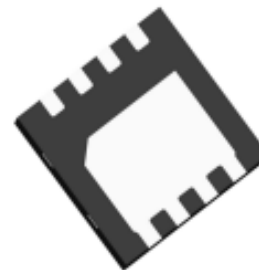
VDS	VGS	RDSON Typ.	ID
30V	±20V	8mR@10V	29A
		10mR@4V5	

➤ Pin configuration



➤ Description

This device uses advanced trench technology to provide excellent RDSON and low gate charge. This device is suitable for use as a load switch or in PWM applications.



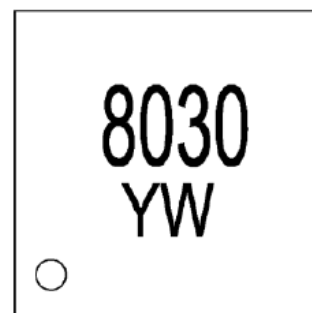
Bottom View

➤ Applications

- Load Switch
- NB/PC
- DCDC conversion

➤ Ordering Information

Device	Package	Shipping
SSC8030GQ4	DFN3x3	5000/Reel



(Y: year/W: week)

Marking



➤ **Absolute Maximum Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain-to-Source Voltage	30	V
V_{GSS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$TC=25^{\circ}\text{C}$	29 A
		$TC=100^{\circ}\text{C}$	22 A
I_{DM}	Pulsed Drain Current ^b	90	A
I_{DSM}	Continuous Drain Current ^a	$TA=25^{\circ}\text{C}$	15 A
		$TA=70^{\circ}\text{C}$	12 A
P_D	Power Dissipation ^c	$TC=25^{\circ}\text{C}$	25 W
		$TC=100^{\circ}\text{C}$	10 W
P_{DSM}	Power Dissipation ^a	$TA=25^{\circ}\text{C}$	3.1 W
		$TA=70^{\circ}\text{C}$	2 W
T_J	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Typical	Maximum	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance ^a		45	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance		6	

Note:

- The value of $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.copper, in a still air environment with $T_A=25^{\circ}\text{C}$. The value in any given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation P_D is based on $T_J(\text{MAX})=150^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

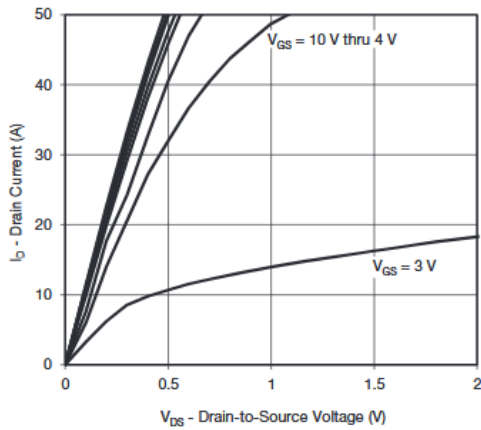


➤ **Electronics Characteristics**($T_A=25^{\circ}\text{C}$ unless otherwise noted)

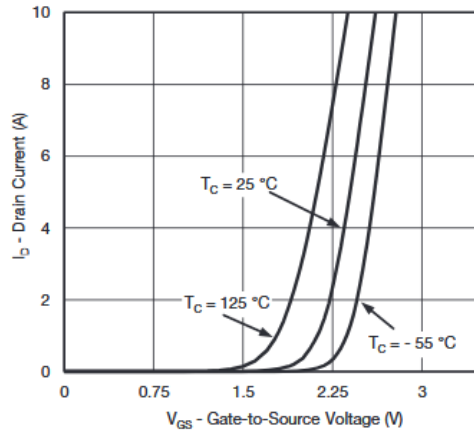
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1		3	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=10V, I_D=15A$		8	11	mR
		$V_{GS}=4.5V, I_D=12A$		10	14	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$			1	μA
I_{GSS}	Gate-Source leak current	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
G_{FS}	Transconductance	$V_{DS}=15V, I_D=12A$		56		S
V_{SD}	Forward Voltage	$V_{GS}=0V, I_S=1A$		0.8	1.5	V
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$		1200		pF
C_{oss}	Output Capacitance			200		
C_{rss}	Reverse Transfer Capacitance			105		
$T_{D(ON)}$	Turn-on delay time	$V_{GS}=10V,$ $V_{DS}=15V, R_L=2.3R, R_G=3R$		18		ns
T_r	Rise time			6		
$T_{D(OFF)}$	Turn-off delay time			70		
T_f	Fall time			17		
Q_g	Total Gate charge	$V_{GS}=10V, V_{DS}=10V, I_D=14A$		20		nC
Q_{gs}	Gate to Source charge			3		
Q_{gd}	Gate to Drain charge			5		



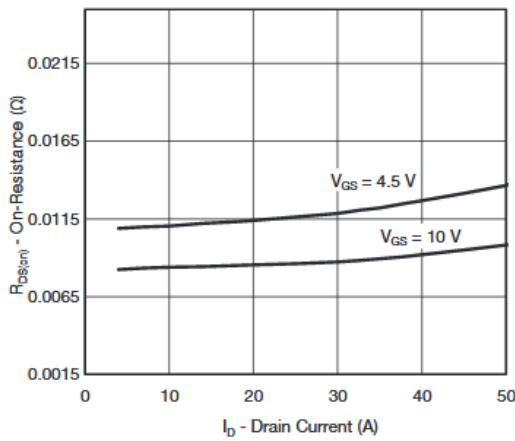
➤ **Typical Characteristics** ($T_A=25^\circ\text{C}$ unless otherwise noted)



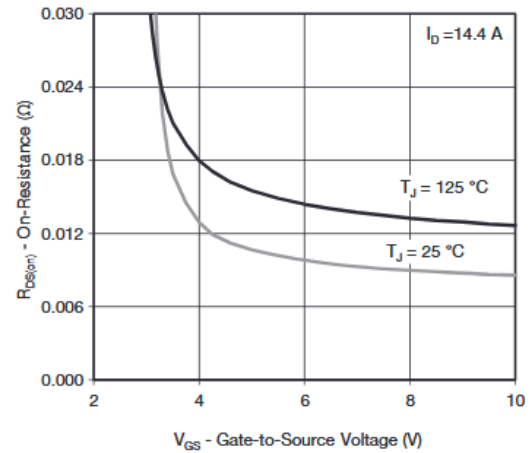
Output Characteristics



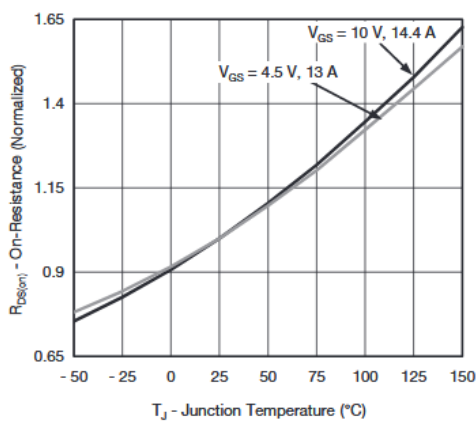
Transfer Characteristics



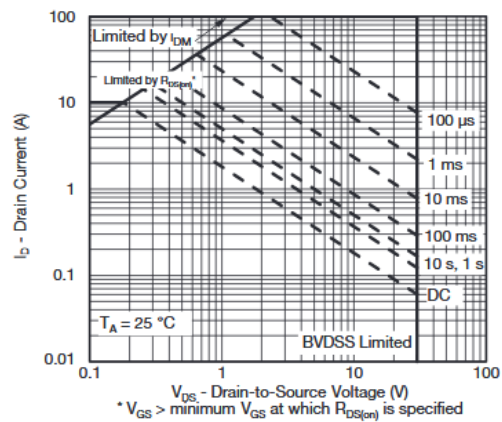
On-Resistance vs. Drain Current



On-Resistance vs. Gate-to-Source Voltage



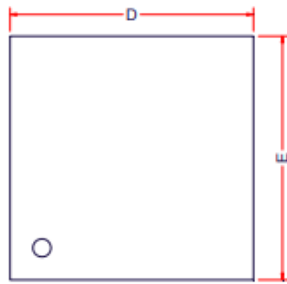
On-Resistance vs. Junction Temperature



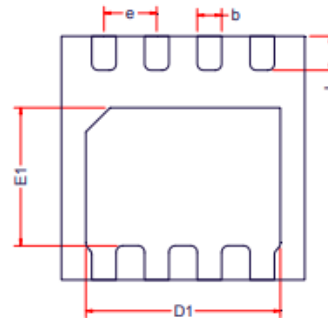
Safe Operating Area, Junction-to-Ambient



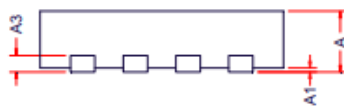
➤ Package Information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

DFN3x3-8L

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.20Ref		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.40	2.45
E1	1.65	1.70	1.75
b	0.25	0.30	0.35
e	0.65BSC		
L	0.37	0.42	0.47

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